

Hardware Unit Test Report

AMP board DC Power Sequence Test

Hardware version	FW version	Sample No.	eMMC Flash P/N
Main Board: V125 AMP Board: V045	BFX-UA300-userdebug 10 QT 19.524.24	AMP Board S/N: YVI0048	Main Board DDR: 1. K4A8G165WC-BCTD 2. K4A4G165WF-BCTD eMMC: KLM8G1GETF-B041 AMP Board NAND Flash: MX30LF4G28AD-TI

1. Test Setup

Equipment:

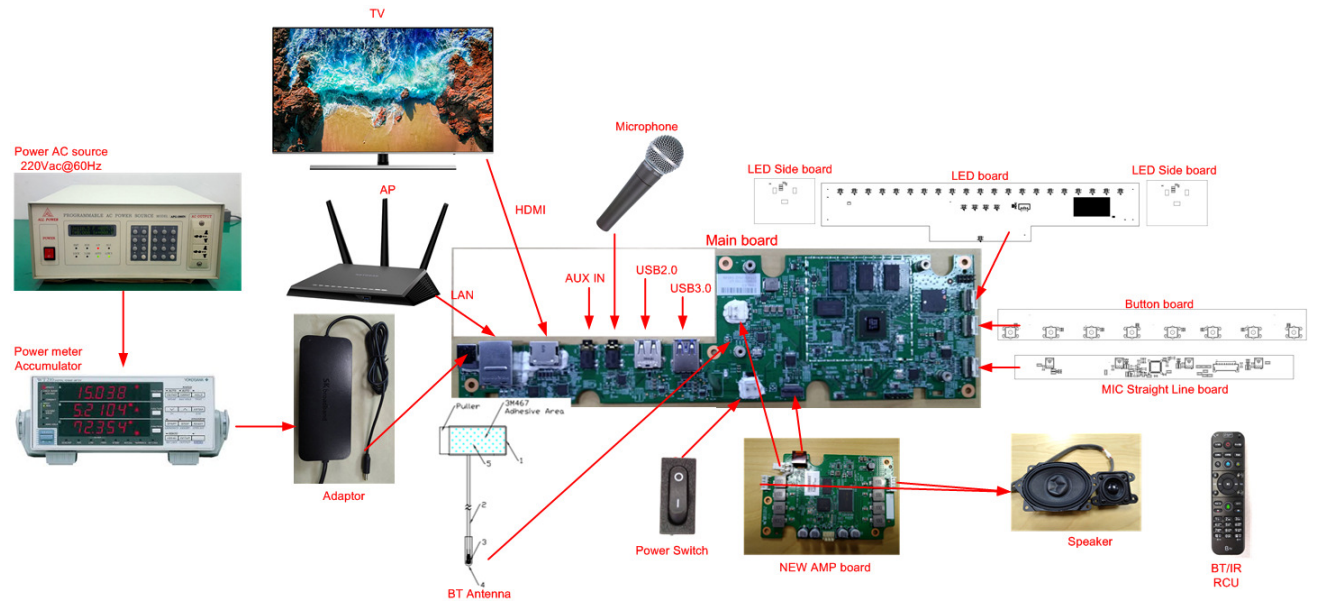
1. BFX-UA300 DVT board V125.
2. AC POWER: APG-1005N: 220Vac @60Hz
3. AC Adapter: LA-A271KS 24V/4A 24V/5A
4. 4K TV: ENVISION P2271WHL
5. Power meter with accumulator: Yokogawa WT210
6. Current probe: TCPA300
7. NETGEAR R7000 1Gbps

Test Environment:

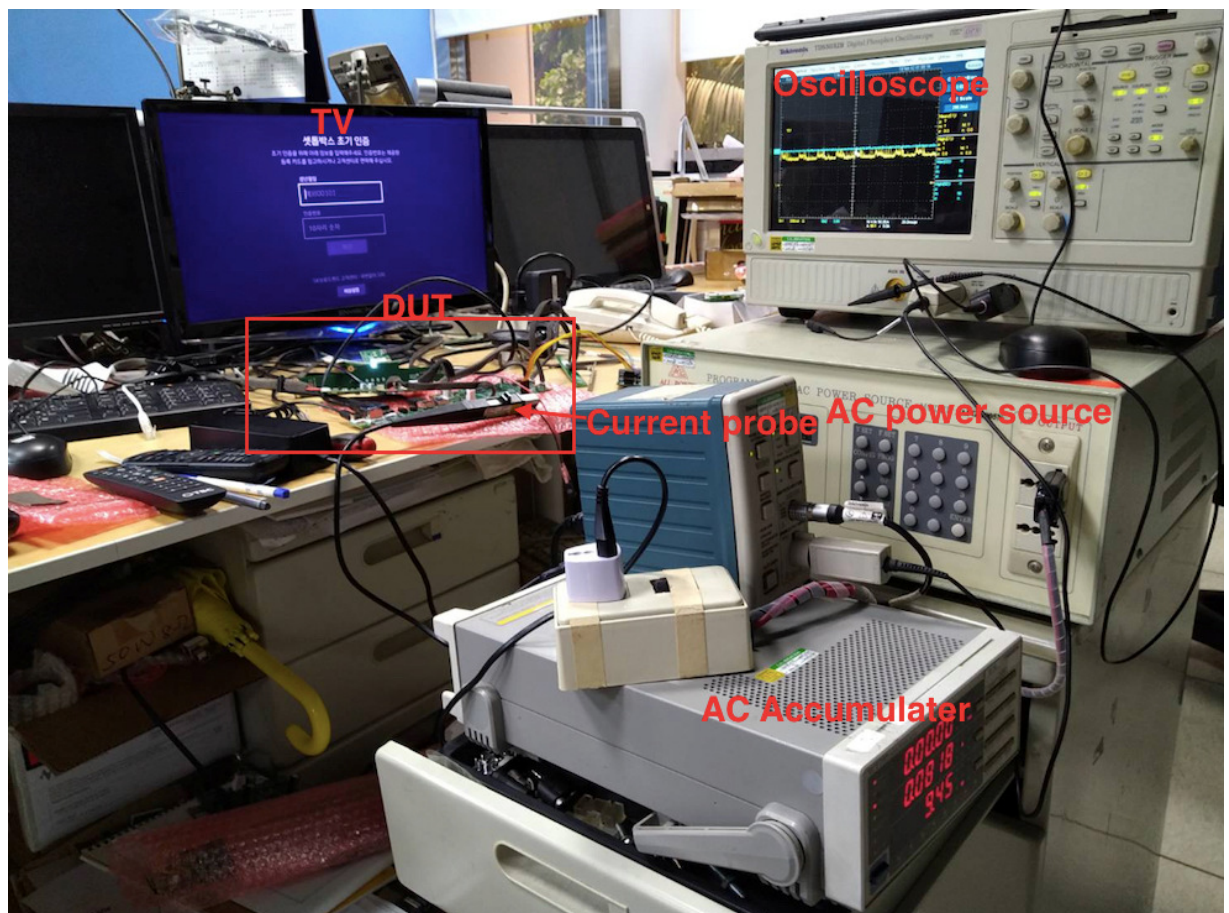
1. Test place: FXN CNSBG Building 1F office
2. Test DUT name: BFX-UA300 DVT V125 board
3. Test environment condition: temperature: 25 deg-C, humidity: 65
4. Test date: 2021/06/01
5. Test result: See section 3 for test results.
6. Test setup picture (block diagram and real test environment picture)

Block Diagram:

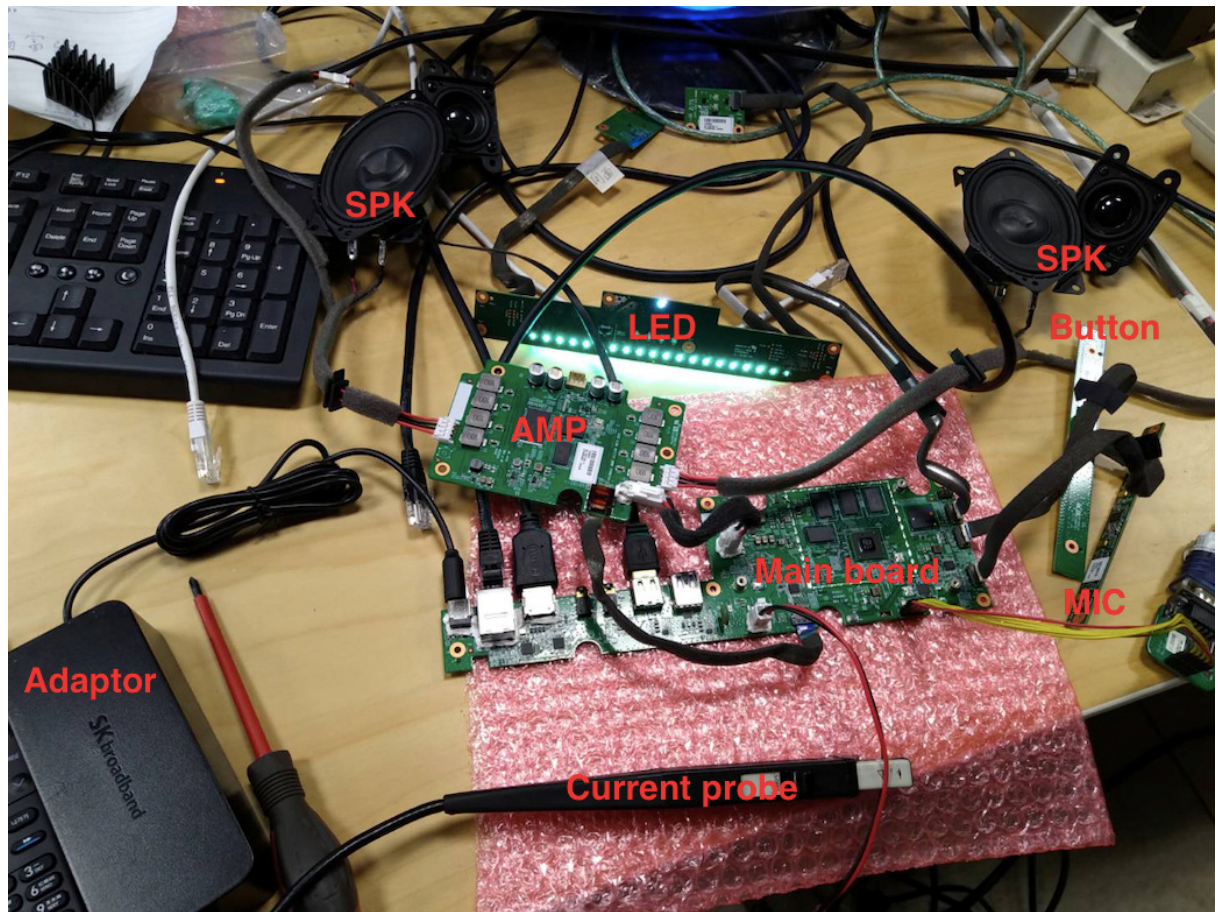
BFX-UA300 AMP board DVT3 DC Power sequence test



Test setup picture:



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2. Test Condition

AC power: 220V@60Hz

DC power: 24V/4A

Connects AC plug of AC-DC adapter to AC power source and DC plug of AC-DC adapter to BFX-UA300. Switch off power switch then switch on to measure the DC power sequence.

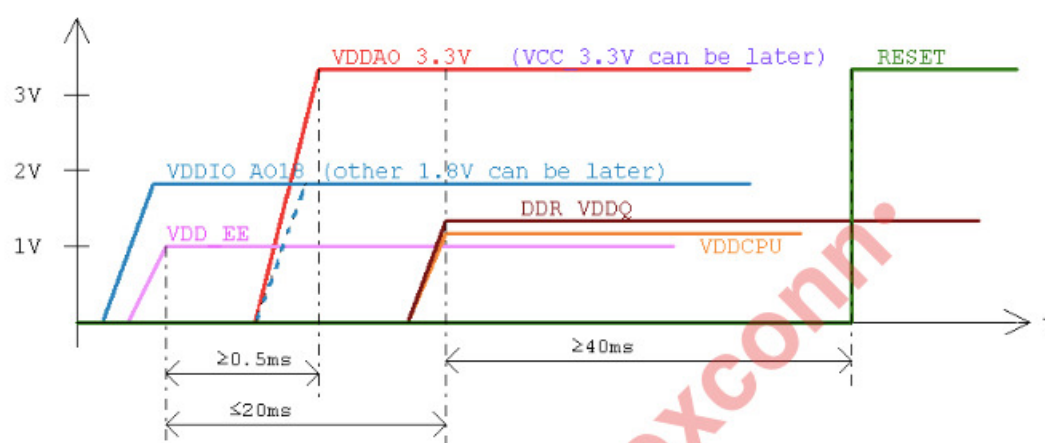
3. Power on specification

As SOC A113X of AMP board, the sequence just follows as spec.

4.9 Recommended Power on sequence

Example power on sequence:

VDD_EE -> VDDIO_AO3.3V & VDDIO_AO18 -> VCC3.3V & VDDIO1.8V & AVDD1.8V -> VDDCPU & DDR_VDDQ



Note:

- 1) VDDIO_AO3.3V & VCC3.3V should ramp up > 0.5ms later than VDD_EE
- 2) All power sources should get stable within 20ms (except for DDR_VDDQ)
- 3) No sequence requirement between IOVREF_18 and VDD_EE
No sequence requirement between VDDCPU & DDR_VDDQ and other power source
- 4) IOVREF (VDDIO_AO18) should ramp up earlier or at the same time with VDDIO_AO3.3V & VCC3.3V. VDDIO_AO3.3V & VCC3.3V should never be 2.5V higher than IOVREF_18.
- 5) In some designs, VDDCPU & VDD_EE are merged to VCC_CORE, the power on sequence should be same as VDD_EE.
- 6) RESET_n should keep low for at least 40ms after power up (except DDR_VDDQ)

Please refer to reference schematics.

4. AC Power on Result and Picture

Test Item	Test Result (ms)	Figure	Spec. (ms)	Pass/Fail
VDD_EE vs VDDAO_3.3V	2.074	Fig.1	≥ 0.5	Pass
VDD_EE vs VCC3.3V	4.181	Fig.2	≤ 20	Pass
VDD_EE vs VDDCPU	5.503	Fig.3	≤ 20	Pass
VDD_EE vs VDDQ1.35V	2.761	Fig.4	≤ 20	Pass
VDDCPU vs Reset	246.2	Fig.5	≥ 40	Pass

Note:

*: A113X vendor - AMLOGIC said the VDDIO_AO18 is no timing limit. So the sequence is ok as currently setup.

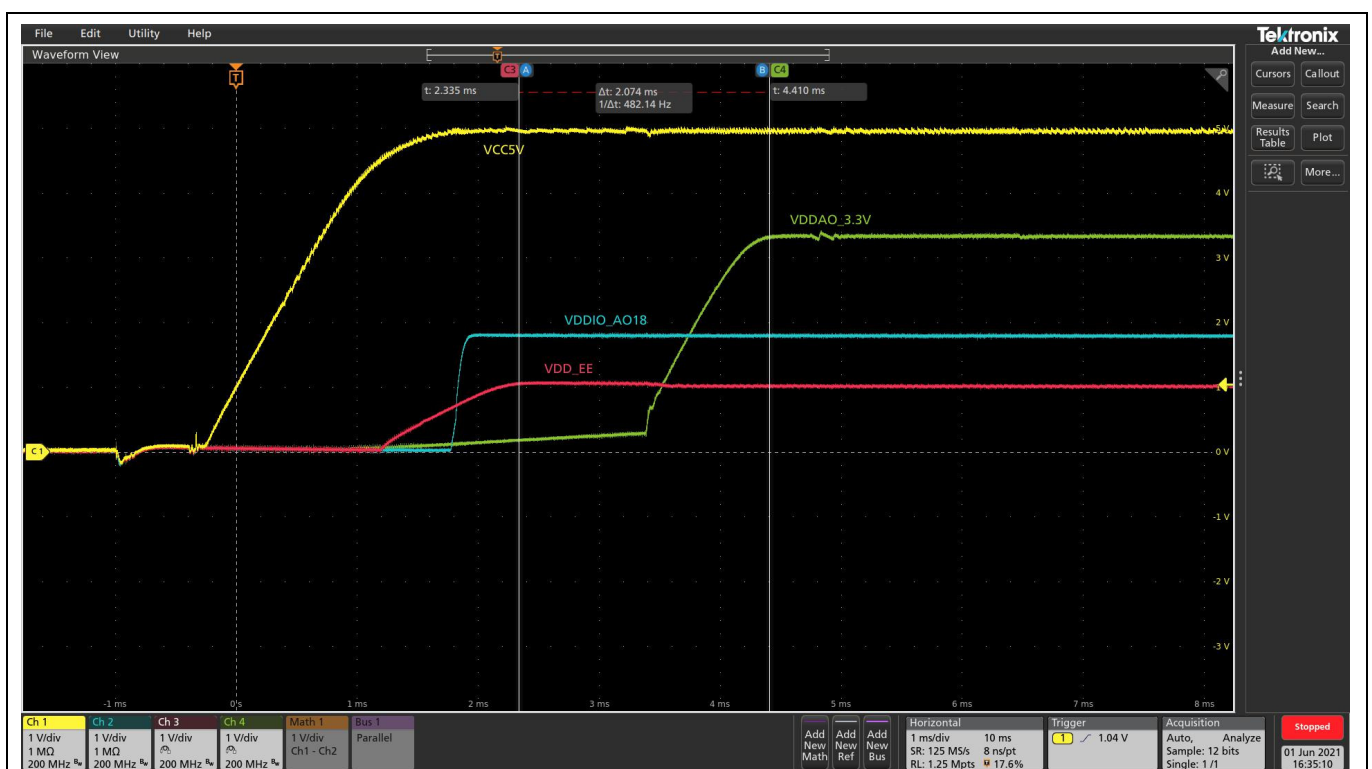


Fig. 1: VDD_EE vs VDDAO_3.3V

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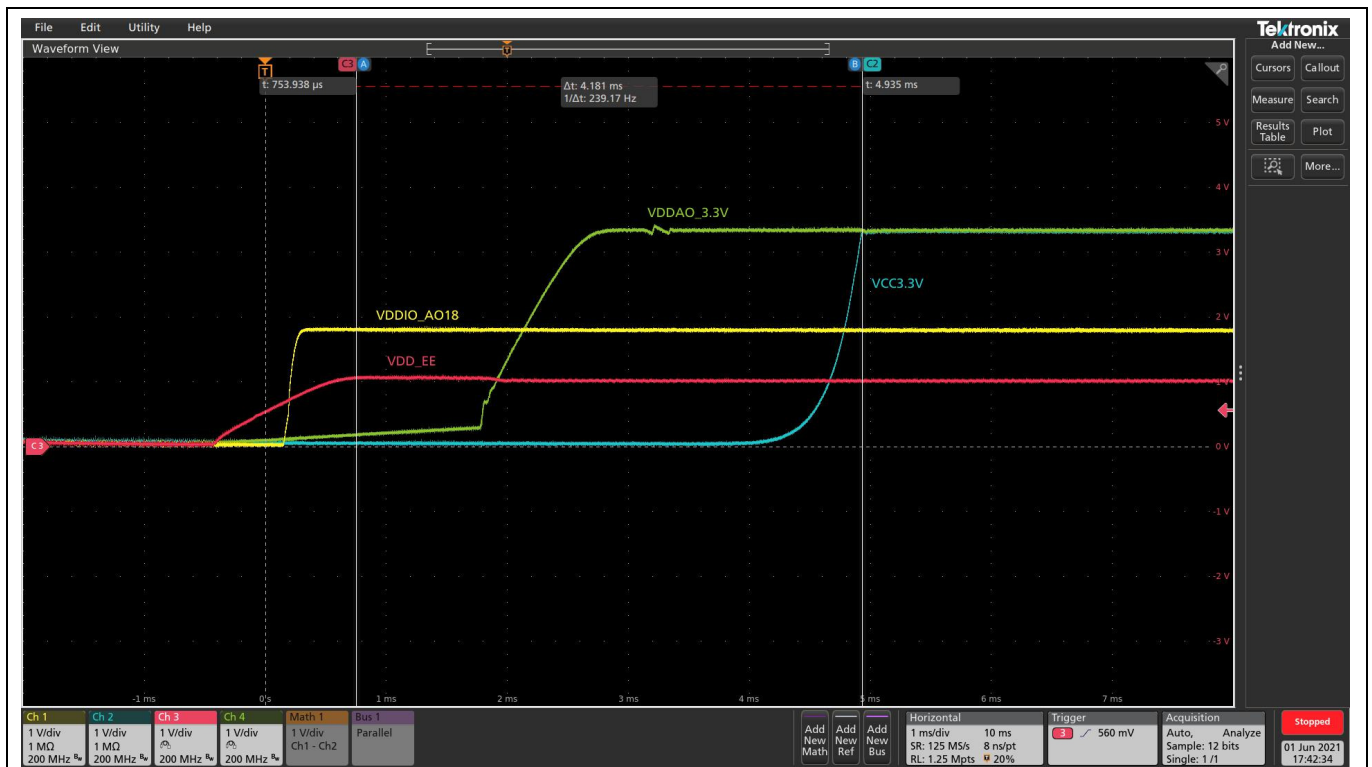


Fig. 2: VDD_EE vs VCC3.3V



Fig. 3: VDD_EE vs VDDCPU

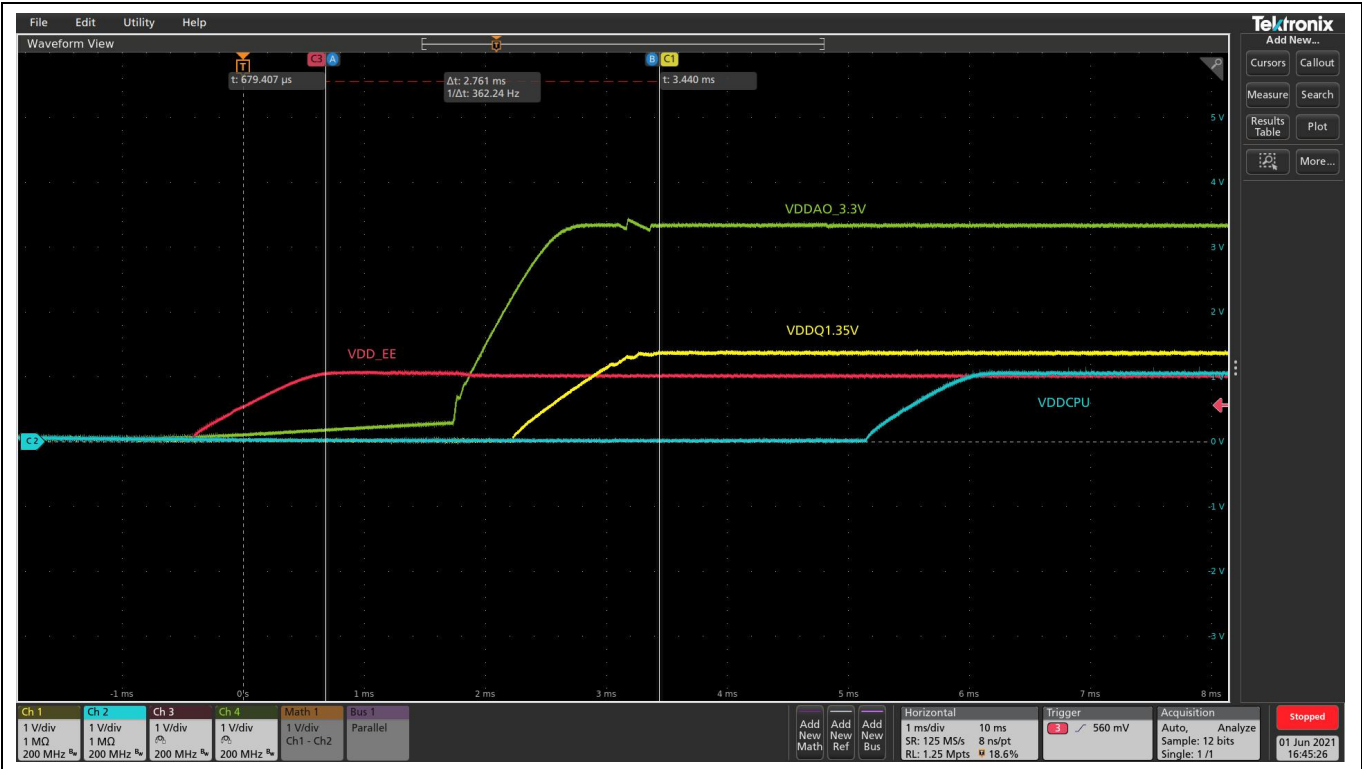


Fig. 4: VDD_EE vs VDDQ1.35V

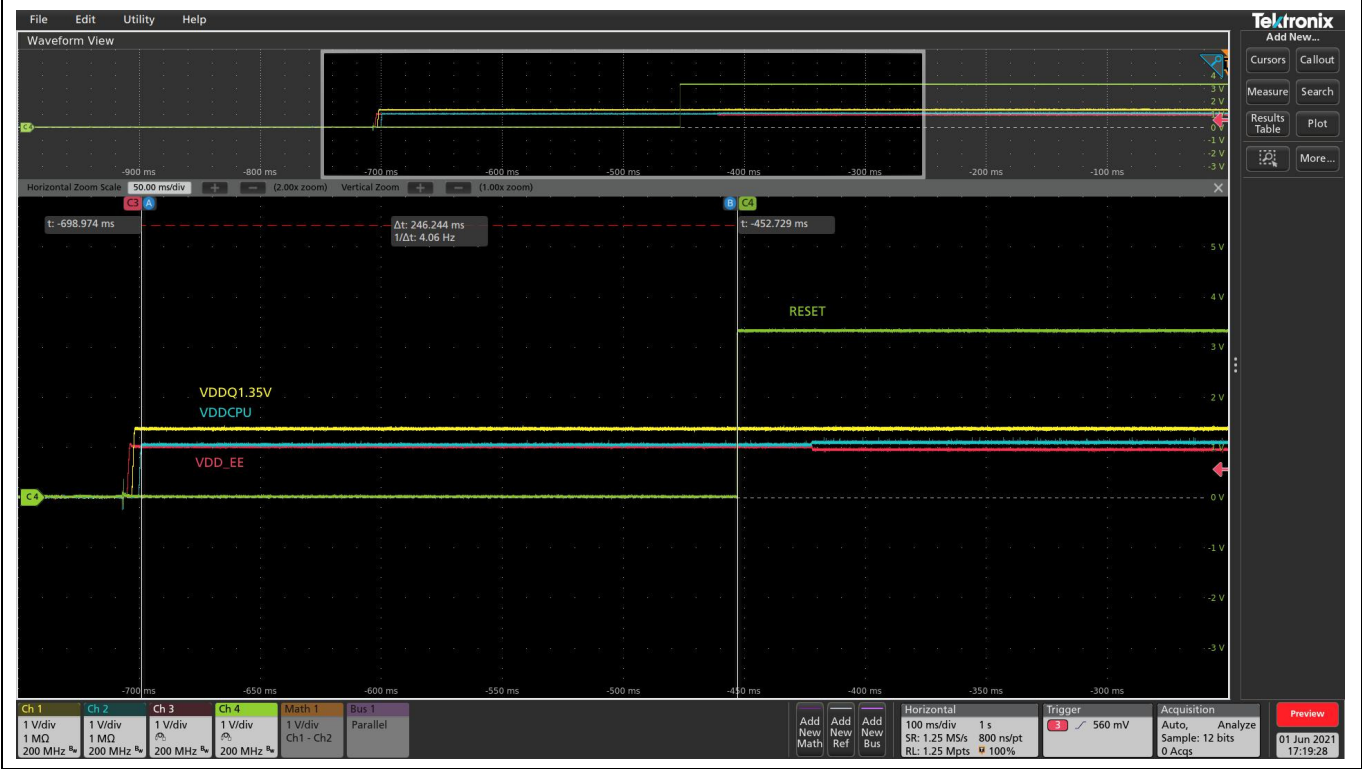


Fig. 5: VDDCPU vs Reset